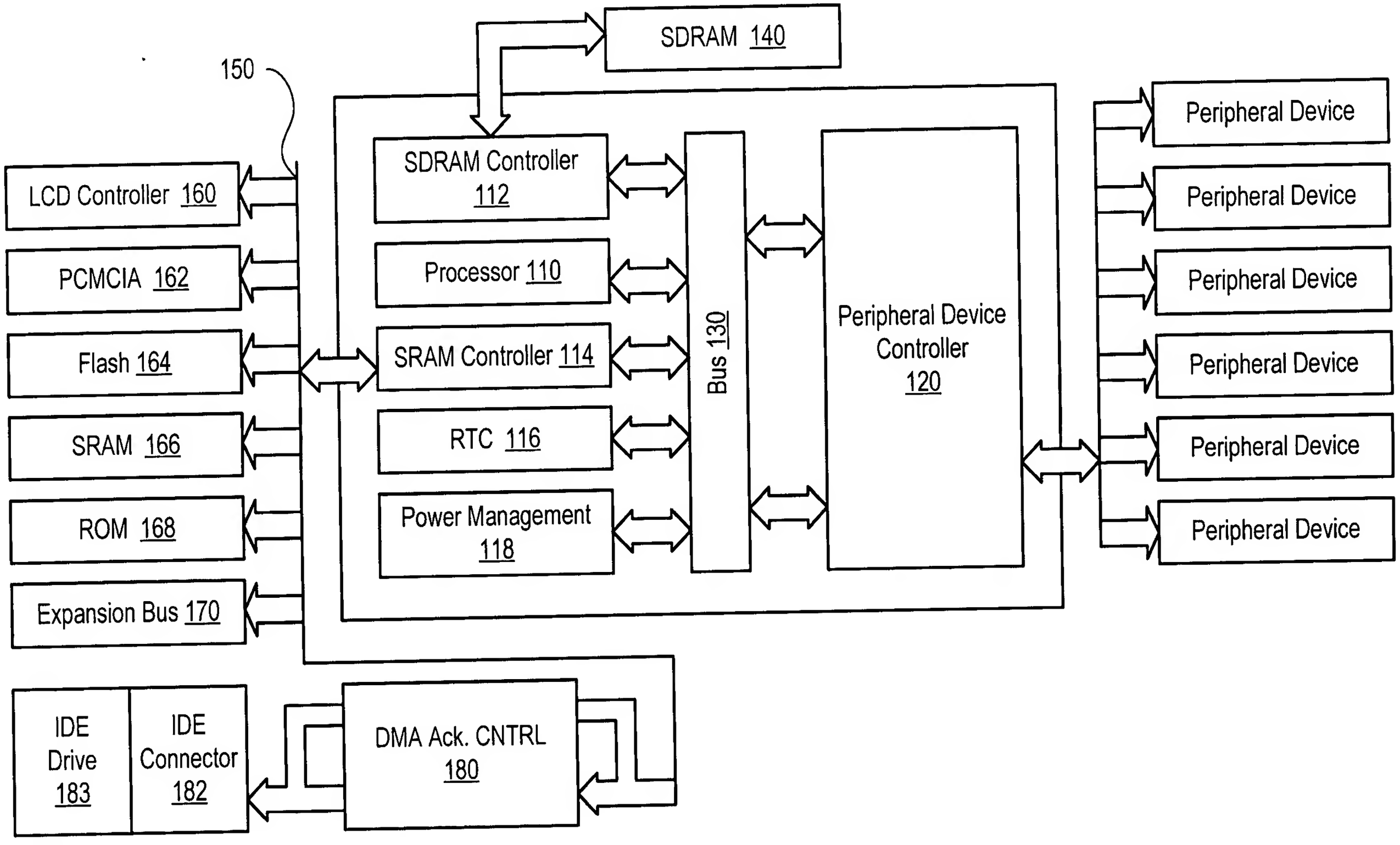
150
SDRAM 140
LCD Controller 160
PCMCIA 162
Flash 164
SRAM 166
ROM 168
Expansion Bus 170
SDRAM Controller 112
Processor 110
SRAM Controller 114
RTC 116
Power Management 118
Bus 130
Peripheral Device Controller 120
Peripheral Device
Peripheral Device
Peripheral Device
Peripheral Device
Peripheral Device
Peripheral Device
IDE Drive 183
IDE Connector 182
DMA Ack. CNTRL 180

Figure 1

DMA Mode Signal Connections

Processor Signal		IDE Drive Signal
$\overline{\text{RESET_OUT}}$	→	$\overline{\text{RESET}}$
RAD[2:0]	→	DA[2:0]
RD[15:0]	↔	DD[15:0]
$\overline{\text{PIOW}}$	→	$\overline{\text{DIOW}}$
$\overline{\text{PIOR}}$	→	$\overline{\text{DIOR}}$
$\overline{\text{PCE[0]}}$	→	CS1Fx (master)
GPIO[*n*]	←	INTRQ

$\overline{\text{PIOS16}}$ (pull-down)

$\overline{\text{PWAIT}}$ (pulled-up)

$\overline{\text{ROE}}$, $\overline{\text{PCE[1]}}$, $\overline{\text{POE}}$, $\overline{\text{PWE}}$, $\overline{\text{PREG}}$ (not Connected)

Additional Signals

GPIO[4]	←	DMARQ
DMA Ackn. Control	→	DMACK

Figure 2

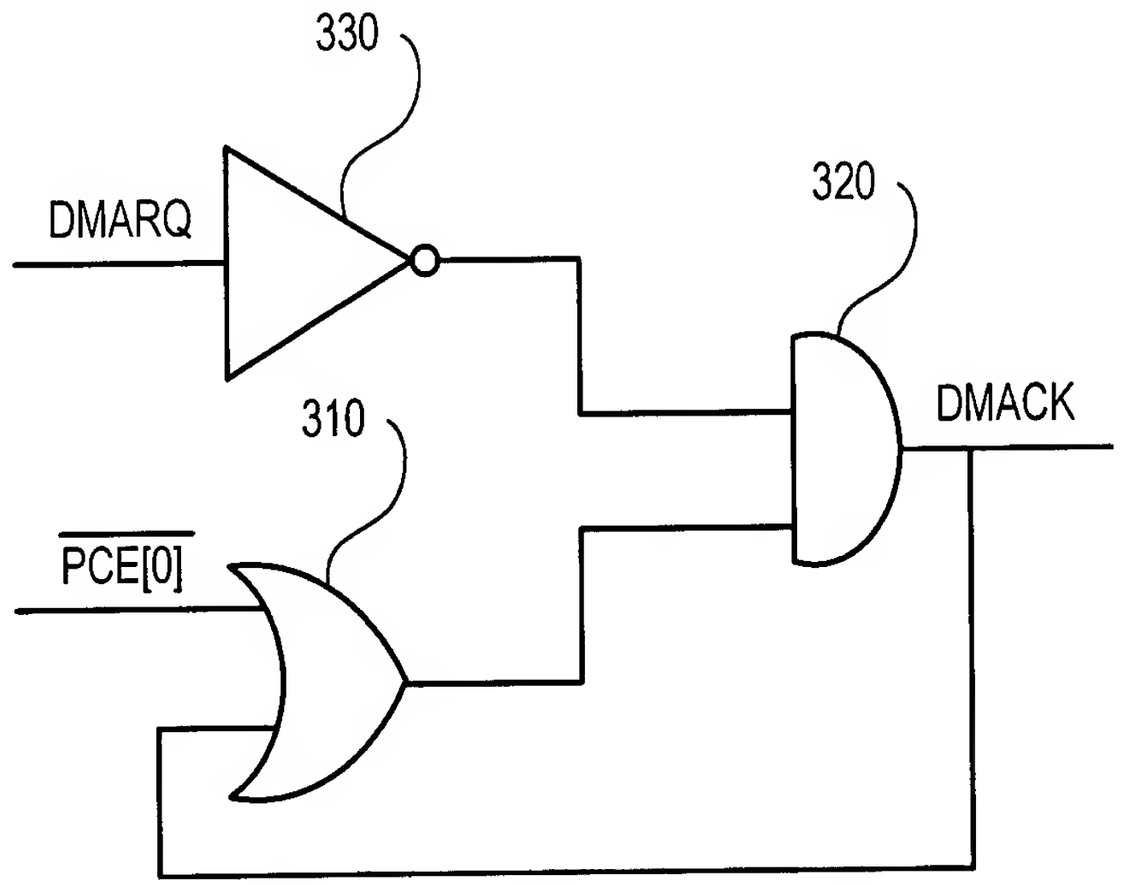

Figure 3

Truth Table for $\overline{\text{DMACK}}$

$\overline{\text{PCE[0]}}$	DMARQ0	$\overline{\text{DMACK}}$
0	0	$\overline{\text{DMACK}}$
0	1	0
1	0	1
1	1	0

Figure 4